AD-A127 153 RESEARCH IN VLSI SYSTEMS(U) STANFORD UNIV CA DEPT OF 1/1
COMPUTER SCIENCE J HENNESSY ET AL. APR 83
MDA903-79-C-0680

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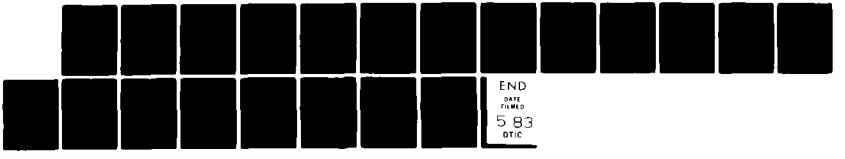

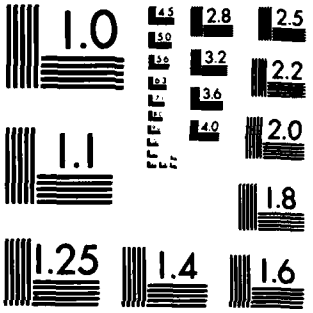

COMPUTER SYSTEMS LABORATORY

DEPARTMENTS OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
STANFORD UNIVERSITY · STANFORD, CA 94305

Research in VLSI Systems

Technical Progress Report for

November 1982 - April 1983

April 1983

Computer Science Department
Computer Systems Laboratory
Information Systems Laboratory
Integrated Circuits Laboratory

This work was supported by the Defense Advanced Research Projects Agency, contracts MDA903-79-C-0680, MDA903-80-C-0432, and MDA-903-80-C-007.

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TECHNICAL STATUS REPORT
November 1982 - April 1983

Research in VLSI Systems
DARPA Contract No. MDA903-79-C-0680
DARPA Order No. 3773
Principal Investigators: J. Hennessy, T. Kailath
Sponsored by Defense Advanced Research Projects Agency
Monitored by P. Losleben

Heuristic Programming Project and VLSI Theory Project
DARPA Contract No. MDA903-80-C-0107
DARPA Order No. 3423
Principal Investigators: E. A. Feigenbaum, B. G. Buchanan, J. D. Ullman
Sponsored by Defense Advanced Research Projects Agency
Monitored by R. Ohlander

A Fast Turn Around Facility for Very Large Scale Integration (VLSI)
DARPA Contract No. MDA903-80-C-0432
DARPA Order No. 3709
Principal Investigator J. T. Meindl
Monitored by D. Adams

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1 REPORT NUMBER: MDA903-79-C-0680(7)	2 GOVT ACCESSION NO.: AD-A127 153
3 RECIPIENT'S CATALOG NUMBER:	
4 TITLE (and Subtitle): Research in VLSI Systems Heuristic Programming Project & VLSI Theory Project A Fast Turn Around Facility for Very Large Scale Integration (VLSI)	5 TYPE OF REPORT & PERIOD COVERED: Technical Status Report Nov. 1982 - April 1983 6 PERFORMING ORG. REPORT NUMBER:
7 AUTHOR(s): J. Hennessy, R. Matthews, J. Newkirk, J. Shott, J. Ullman, H. Brown	8 CONTRACT OR GRANT NUMBER(s): MDA903-79-C-0680 MDA903-80-C-0107 MDA903-80-C-0432
9 PERFORMING ORGANIZATION NAME AND ADDRESS: Computer Science Dept.; Computer Systems, Information Systems, Integrated Circuits Laboratories; Stanford University, Stanford, CA.	10 PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS:
11 CONTROLLING OFFICE NAME AND ADDRESS: Defense Advanced Research Projects Agency Arlington, Virginia 22209	12 REPORT DATE: April 1983 13 NUMBER OF PAGES: 19
14 MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office): Office of Naval Research (Stanford Branch) Stanford University Stanford, California 94305	15 SECURITY CLASS. (of this report): UNCLASSIFIED 15a DECLASSIFICATION/DOWNGRADING SCHEDULE:

16 DISTRIBUTION STATEMENT (of this Report)

Unclassified; approved for general distribution.

17 DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18 SUPPLEMENTARY NOTES

19 KEY WORDS (Continue on reverse side if necessary and identify by block number)

Very Large Scale Integration	Computer Supported FTL
Regular Expression Compilation	Palladio: IC Designer's Assistant
MIPS: A VLSI Processor	Electron Bean Lithography
Relative Layout Tools	Micron CMOS
Graphics Architectures	Wafer FabricationFacility

20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

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S/N 0102-LF-014-6601

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

Research in VLSI Systems

Progress Report for November 1982 - April 1983

April 1983

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Abstract

This report summarizes progress on the DARPA funded VLSI Systems Research Projects from November 1981 to April 1983, inclusive. The major areas under investigation have included: analysis and synthesis design aids, applications of VLSI, special purpose chip design, VLSI computer architectures, signal processing algorithms and architectures, reliability studies, hardware specification and verification, VLSI theory, and VLSI fabrication. The major research problems are introduced and progress is discussed; the Appendix contains a list of published research papers from these projects.

Key Words and Phrases: VLSI, design automation, computer-aided design, special purpose chips, VLSI computer architecture, signal processing, routing, layout, memory reliability, VLSI theory, knowledge-based design systems, IC fabrication.

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Executive Summary

The major progress of note for this period is as follows:

1. *MIPS: A VLSI Processor.* MIPS (Microprocessor without Interlock between Pipe Stages) is a project to develop a high speed (> 1 MIP) single chip 32-bit microprocessor. During this last period the processor design was completed and submitted to a March MOSIS run.

2. *TV: An nMOS Timing Analyzer.* TV and IA are timing analysis programs for nMOS VLSI designs. Based on the circuit obtained from existing circuit extractors, TV determines the minimum clock duty and cycle times. TV was developed during this six month period and used heavily in the MIPS project.

3. *Palladio: An IC Designer's Assistant.* The Palladio system is a framework for experimentation with circuit design methodologies, knowledge-based expert system design aids and rule-based symboloic simulation concepts. During the past six months Palladio's basic system structure was refined, the rule-based simulator was extended and a prototype expert system for interconnect mask level assignment was implemented.

4. *Computer Support - FABLE.* We have completed a prototype of a wafer fabrication description language called FABLE [Ossher 83] which will allow us to produce electronic run sheets which will guide a technician through the fabrication sequence or, ultimately, contol an automatic fabrication facility. A key feature of this language is the separation of the high level process step specification from the equipment-specific detailed execution of these high level steps to enhance the protability of a process specificiation in space or time.

5. *Computer Support - Hardware.* We have installed a VAX 11/750 in the Fast Turn-Around Laboratory which has an Ethernet link to the other DARPA VLSI computers on campus. Initial efforts to couple this VAX to wafer fabrication equipment have concentrated on a serial link which allows us to down-load reticle, stepping, alignment, and exposure information to to an Ultratech 900 wafer stepper.

6. *Electron Beam Lithography.* The Stanford MEBES machine has passed on-site acceptance and has been used to write several masks sets for the Fast Turn-Aound Laboratory including masks for the Geometry Engine [Clark 80] with both 3.0 μ and 4.0 μ minimum features. Additionally the machine has been retrofitted with a lanthanum hexaboride (LaB_6) electron gun which provides a minimum spot size of 1/8 μ and a 4X improvement in current density for use with high resolution, low sensitivity resists.

7. *NMOS Wafer Fabrication.* The Fast Turn-Around Laboratory has been starting approximately 3 NMOS or CMOS runs per month with 3.0 μ and 4.0 μ feature sizes. The largest design fabricated to date has been the Geometry Engine [Clark 80] which is presently awaiting the results of functional testing.

8. *2 Micron CMOS.* Test devices using Stanford's 2 μm CMOS process have been fabricated and tested. This process features a 4 μm n-well and a 400 Angstrom oxide thickness. E/D NMOS devices on the same wafers allow direct performance comparisons between 2 μ CMOS and NMOS technologies. Test results indicate that drain-induced barrier lowering (DIBL) is one of the most severe limits to the further scaling of this technology.

9. *Deep Trench Isolation Technology.* We have begun an investigation of deep trench isolation techniques as a means of increasing the packing density of CMOS while reducing latch-up sensitivity. Anisotropic plasma etching has resulted in isolation grooves 1.7 μ wide and 4.0 μ deep. We are presently investigating the fixed-charge properties of these isolation sidewalls to understand the potential parasitic leakage paths which may exist in this technology.

10. *LPCVD Deposition of Tungsten.* We have been investigating the use of W-LPCVD for use as both a contact and an interconnect metallurgy in high density integrated circuits. We have achieved both selective (i.e. deposition only on exposed silicon) and non-selective depositions of tungsten.

Technical Progress

1 Design Description, Analysis, and Synthesis

1.1 Silicon Compilation

We are experimenting with a more powerful state assignment algorithm for coding states of nondeterministic automata. The regular expression compiler generates state information for a nondeterministic finite automaton, input and output signal information, and information about what states *conflict*, in the sense that it is possible for both to be on at one time. We then wish to code the states so that the presence of any state can be recognized, regardless of what other states are on at the same time. A simple heuristic was implemented last year; for example, it generates essentially the Mead-Conway PLA for the traffic light controller, when given a regular expression describing the action of that controller. However, on larger examples, it can be less than optimal. We are exploring more complex algorithms for selecting codes, and have almost finished the implementation of an algorithm that combines optimal packing of codes for small sets of states with a "min-cut" heuristic for partitioning problems involving large sets of states.

In the initial stages of design is a true "silicon compiler," one that will take a reasonable subset of Pascal and produce layouts that we hope will have performance comparable to that of hand designs. We plan to avoid what appears to be a trap in silicon compilation of high level languages: making every chip look like a microprocessor. Our intent is to rely heavily on existing optimization tools for Pascal, but also to write a compiler that is prepared to invent appropriate bus structures and more general interconnection networks.

Staff: H. Trickey, A. Karlin, J. Ullman.

References: [Trickey 83]

1.2 TV - An nMOS Timing Analyzer

TV and IA are timing analysis programs for nMOS VLSI designs. Based on the circuit obtained from existing circuit extractors, TV determines the minimum clock duty and cycle times. It calculates the direction of signal flow through all transistors before the timing analysis is performed, in contrast to combinations of designer-assisted and dynamic determination of signal flow, as in Crystal, being done at Berkeley. The timing analysis is breadth-first (block-oriented) and pattern independent, using only the values *stable*, *rise*, *fall*, as well as information about clock qualification. Its running time is linear in the number of nodes and transistors, and can analyze 4,000 transistors per minute of VAX 11/780 CPU time.

IA (TV's Interactive Advisor) allows the user to quickly experiment with ways to increase circuit performance. With the IA, the user can resize pull-ups and pull-downs or insert super buffers, and find out the effects of these changes on chip-wide performance interactively. By using information already computed by TV, it is able to propagate the effects of changes through 1,000 transistors per second of VAX 11/780 CPU time.

TV was heavily used in the MIPS project. When TV was run on the first version of MIPS, it predicted a cycle time four times longer than our original design goal. By making extensive modifications to the design we were able to reduce the cycle time to half the original prediction.

Accuracies within in 20% for most critical paths compared to circuit simulation and fabricated chips have been achieved.

Staff: N. Jouppi

Related Efforts: Crystal (Berkeley)

References: [Jouppi 83]

1.3 Palladio: An IC Designer's Assistant

The Palladio system is a framework for experimentation with circuit design methodologies, knowledge-based expert system design aids and rule-based symbolic simulation concepts. The goal of the project is to develop an experimental integrated design environment to assist in the full design, test and debug cycle.

During the past six months we have rewritten major parts of the Palladio framework code making it more robust. We have concentrated on a clean implementation of those parts of the system which have proven useful, and we have eliminated those parts which were marginal. One improvement has been the user interface. All user interaction with the system is now via the mouse, except for the entry of textual information and the handling of exceptional conditions.

We have continued our work on a mixed level, rule-based simulator. The simulator is independent of any particular level of circuit specification. The primary idea is to exploit hierarchical design descriptions to help manage the simulation of complex systems. The simulator can be used to perform symbolic simulation and goal-directed simulation. During the past six months we have tuned the simulator and extended it to handle arbitrary sequential circuits. The system has been interfaced to a high-resolution color display, and the simulator can now produce dynamic logic-level simulation "*cartoons.*"

We have implemented a prototype rule-based expert system which determines the mask levels of the interconnections for a "black wires and cells" MOS circuit specification. The rules take into account the estimated lengths of the wires, the mask levels of the interconnected ports, the electrical characteristics of the mask levels, and the types of signals on the wires. The expert system resolves wire intesection conflicts by tradeoffs between prefered mask levels, the cost of resolving the conflict by inserting vias, and overall circuit performance. During the next six months we plan to augment the system's knowledge base so that it does transistor gate sizing concurrently with the interconnection mask level assignment.

Our work on developing a uniform internal reprsentation of a design specification continues. This repsentation serves as the basis for knowledge-based systems which can reason about a design in order to assist in the refinement of abstract specifications to more detailed implementation specifications. This work has involved research on models of the design process which reflect design goals, design alternatives and design tradeoffs.

Staff: H. Brown, G. Foyster, N. Singh (Stanford and Fairchild), C. Tong, J. Yan

References: [Brown 82, Foyster 83]

2 VLSI Processor Architecture

2.1 MIPS - A High-Speed Single-Chip VLSI Processor

MIPS (Microprocessor without Interlock between Pipe Stages) is a project to develop a high speed (> 1 MIP) single-chip 32-bit microprocessor. Like the RISC project at Berkeley, MIPS uses a simplified instruction set and is a load-store architecture.

The MIPS architecture is summarized in previous technical progress report and is discussed in several publications. During this six months we received and tested the MIPS' test chips. Using this test data, we made minor changes. We then completed the entire design, spent approximately 3 months in design and performance verification and submitted the first complete version of the processor to MOSIS. The project experience in chronicled in [Hennessy Jouppi83 83].

Staff: J. Gill, T. Gross, J. Hennessy, N. Jouppi, S. Przybylski, C. Rowen.

Related Efforts: RISC (UCB), IBM 801 (IBM Yorktown), Cray-II (Cray Research).

References: [Hennessy Jouppi 81, Hennessy Jouppi83 83, Hennessy Gross 83, Gross 83]

3 Theoretical Investigations

Alan Siegel has made further progress on the "offset" problem for river routing, i.e., finding the best relative placement for two modules that are to be wired across a channel. He has a set of simple axioms that wiring rules must satisfy (an example of a "wiring rule" is the requirement that wires run horizontally, vertically, or along a 45-degree diagonal) in order that the offset problem can be solved by a fast algorithm.

He has also examined the "bristle blocks" problem discussed by Leiserson and Pinter, where instead of one module we have two rows of rigid modules. Wiring rules meeting his conditions, as any reasonable rule will, can have the bristle blocks problem solved by an equally efficient algorithm. However, the generalization, where we try to wire together an arbitrary number of rows of modules, is NP-complete.

Staff: A. Siegel.

Related Efforts: Leiserson and Pinter (MIT).

References: [Siegel 83]

4 Fast Turn-Around Laboratory

This section describes recent progress in the Fast Turn-Around Laboratory (FTAL) at Stanford University. Areas to be covered include:

1. The incorporation of computer support into the wafer fabrication facility to allow better control and reporducibility of both production and device/materials research activities.

2. Recent results in the area of high resolution microlithography. Specifically, we will report on results obtained from the use of a MEBES electron beam lithography system for use in both mask making and direct-write lithography applications.

3. Progress in wafer fabrication and device research including the fabrication of the Geometry Engine with 3 μ minimum feature sizes and the development of a 2 μ CMOS process.

4. Advances in interconnection and contact technology including LPCVD deposition of tungsten and plasma techniques for wafer planarization.

Work done in within the FTAL in the area of electrical device testing and characterization is included in the Testing section of this document.

4.1 Computer Support

Initial activities in providing computer support to the Fast Turn Around Laboratory generally fall in the category of planning, preparation, and design. We have established contact with key researchers involved in the use of computers in wafer fabrication facilities at Hewlett-Packard, Xerox, DEC, Sandia, and IBM. This has enabled us to get a clear view of the current state of the art and, more importantly, has enabled us to develop a strategy which will allow us to advance the field of computer support in wafer fabrication activities - particularly in a low volume research/production environment such as the FTAL.

In our view, one of the keys to establishing powerful and versatile computer support of a wafer fabrication activity is to develop a *language* capable of representing both a fabrication process and a fabrication facility. We have completed an initial design of this language, FABLE [Ossher 83], and are presently refining it by manually coding a variety of existing process sequences to assess the power and flexibility of this language. In order to enhance the transportability of a FABLE fabrication sequence, we are endeavoring to separate the high level description of the process steps in a fabrication sequence (the *run sheet*) from the detailed equipment-specific description of *exactly* how each step is executed in a particularly laboratory (the *line model*). This separation of the high level run sheet from the equipment-specific line model greatly enhances the portability of a process description in the same way that a compiler allows a program written in a high level language to be run on machines of widely varying architecture. A key feature of the development of FABLE is the critical scrutiny which is is receiving from both fabrication technologists and programming language researchers.

In parallel with the development of the FABLE system, we are establishing a computer hardware base within the wafer fabrication facility of the FTAL. Specifically, we have installed a VAX 11/750 running under Unix and have connected it to the Ethernet which couples to the other campus Computer Science and VLSI research computers. Additionally, we are presently installing a 420 MByte system disk and have connected terminals to the system in a number of key locations in the laboratory. Very early efforts to establish the VAX as the central data base for all aspects of wafer fabrication activity include serial RS232 interface links between both the Ultratech mask aligner and the parametric test system. We are presently able to down-load reticle, alignment, stepping distance, and exposure intensity information from the VAX to the Ultratech 900 Stepper.

4.2 Microlithography

MEBES had been installed at the start of this period and work with Perkin-Elmer E.B.T. has been going on for acceptance of the standard machine. In July we prepared job and pattern files for a CHMOS mask set for our Canon FPA 141 4X projection aligner and then went to P-E to write the 12 mask levels in reticle mode. The 1X die size was 12.5 by 12.5 mm and took about 11 minutes each to write on a MEBES very similar to ours. At the same time, we learned more of the fine details in processing PBS E-beam plates.

We accepted the standard MEBES machine on 22 September, 1982. Work on the Lanthinum hexaboride (LaB_6) gun retrofit contract with P-E was started in early October. Besides the gun itself, which will enable the column to achieve an 0.125 micron spot size and larger exposure currents at spot sizes of 0.25

to 1.0 microns, the major component added to the MEBES is an MEBES II electron source control. The first LaB_6 gun installed was in early November and changes were made for it thru December. By mid-December, most of the work was on new software to support this new hardware, and recalibration of the entire system. During this time we studied the software on MEBES for writing job files and manipulating pattern files. For example with a new program from P-E called "Unify" there are now 3 ways to bloat the geometries of a pattern file and 2 ways to do a shrink. These we will investigate to see which one is "best" in differing situations.

Specifications for the new Ultratech 900 aligner reticles were studied, and after dialogues with Ultratech, we prepared job and pattern files for a complete reticle set including all alignment marks and a scaled primary pattern - the Geometry Engine with 3 micron minimum features. The die at this scale is 6879 by 6085.5 microns, three of which would fit into one Ultratech field. We also learned by visits to Ultratech the technology to mount pellicles onto the 3 by 5 inch reticles and then to attach the reticle guides for loading into the Ultratech 900.

Work on the tri-level resist process for direct write E-beam continued jointly with P-E. To get the process working we investigated several RIE plasma systems for the anisotropic etch of the bottom polymer planarization layer. Of all research systems, the RIE-51 from Materials Research Corp seemed the most flexible. The major problem was the formation of silicon or other "grass" during the anisotropic polymer etch. Some of the grass was determined to be from metals sputtered from the stainless steel electrodes. A teflon electrode shield has since been incorporated to reduce this potential source of contamination. Typical operating conditions for the polymer etch were:

1. Pressure: 5 - 10 mtorr

2. Power: 75 watts over 6 inch diameter electrode

3. Gas flow: 15 sccm oxygen, no CF4

4. Electrode spacing: 3 cm

E-beam exposure of the top level of the tri-level structure coupled with anisotropic RIE etching of the planarization layer have resulted in 0.5 μ lines and spaces in 1.2 μ thich films of AZ 1470 resist.

Several projects from J. Newkirk and R. Matthews design class which had been converted from CIF to MEBES format by ISI were sent back to Stanford by network. The pattern files then had to be transferred to MEBES by 9-track tape. While gaining experience in transferring pattern files from a DEC-20 to the DG S-250 (the control computer for MEBES) we became convinced of:

1. The desirability of connecting the MEBES machine to the Ethernet to eliminate the handling of 9-track tapes.

2. The desirability of having in-house CIF to MEBES conversion capabilities. Efforts are underway, with valuable aid from ISI, to bring up portions of the MOSIS software at Stanford.

4.3 Wafer Fabrication and Devices

4.3.1 NMOS Wafer Fabrication

During previous reporting periods, the wafer fabrication activity of the Fast Turn-Around Laboratory had concentrated on the installation and characterization of *individual* pieces of wafer fabrication equipment. During this period, we have shifted our attention to the *integration* of all of these process steps to allow of us fabricate a variety of complete devices and circuits including the Geometry Engine [Clark 80] with both 3 μ and 4 μ minimum feature sizes. Additionally, we have more fully exercised the capabilities of our laboratory by initiating an average of 3 runs per month.

Using E-beam masks which written, developed, and etched at Stanford, we have been characterizing our NMOS process in order to determine the appropriate amount of "sizing" (bloats and shrinks) to be included in each mask so that we deliver feature sizes which match the *as drawn* feature sizes specified by the designer. Using both optical and electrical line width measurements we a standard deviation in final line width of $\sim$0.1-0.15 μ across the wafer for diffusion, poly silicon, and aluminum lines. We do not yet have sufficient statistics to specify our run-to-run line width variation.

Using our Canon FPA 141 4:1 optical projector, we have recently completed two runs of the second generation of the ZnO/Si SAWFET and one run of the 40,000 transistor Geometry Engine using 4.0 μ minimum feature sizes. Test stripes on the Geometry Engine are fully functional and we are presently awaiting the results of functional testing.

More recently, we have initiated, and nearly completed, fabrication of two runs of the Geometry Engine using the Ultratech 900 1:1 wafer stepper and 3.0 μ minimum feature sizes. These runs represent the first two "real" runs which have been initiated using the Ultratech and are de-bugging the process of using the MEBES machine to produce 1:1 reticles which are suitable for the auto-alignment, auto-focus system on the Ultratech.

4.3.2 High Density CMOS

We have completed several successful runs of our 2 μ n-well CMOS process. This process features 400 Angstrom gate oxides, a 4 μ deep n-well, and "low DT" processing resulting in n^+ and p^+ source/drain junction depths of 0.3 μ and 0.55 μ, respectively. These devices show good leakage performance for low V_{GS} and crisp inverter characteristics for n- and p-channel devices with $Z = L = 2$ μ. Latch-up characterization of these devices is in progress at this time.

4.3.3 Device Research

As an extension to the 2 μ CMOS development program, we have begun a study of the use of p-channel depletion loads in an enhancement/depletion logic configuration. This particular configuration seems to offer an interesting compormise in speed vs. power vs. packing density when compared to either conventional enhancement/depletion NMOS or static CMOS configurations. More specifically, a p-channel depletion device ($V_T \sim +1.0$ V) provides a nearly ideal load line characteristic with its drain tied to its source because there is *no body effect*. This approach offers a density advantage in comparison to static CMOS designs, for example, because it requires only one load element per logic gate without requiring the more complex clocking requirements of clocked CMOS techniques. A more detailed comparison of E/D NMOS, static CMOS, and E/D CMOS is in progress.

4.3.4 Deep Trench Isolation

An effort has been started to investigate deep trench isolation for improving the packing density of CMOS layouts. Initial plasma etching results look very promising and will be pursued to understand the limits of this technology.

The effective scaling of bulk CMOS is limited by the n^+-p^+ spacing, which for our present 2 μ CMOS process is a minimum of 8 μ. With present local oxidation isolation technologies, the reduction of this spacing is limited by latch-up and breakdown considerations. Deep trench isolation promises to reduce this spacing to the range of 1 to 2 μ. Using this technique which has been applied only to CMOS on epitaxial layers a deep trench or groove is etched through the epi layer into the Si substrate. The trench is then filled with an insulator and then back etched to provide a near-planar surface for the rest of the process. With this process source/drain diffusions can be butted up against the trench to give an n^+-p^+ spacing equal to the trench width.

Our initial efforts have concentrated on the etching of the trenches. To do this two plasma etchers have been used. For the first stage a Branson oxide etcher was used to anisotropicaly etch through a 7000 Angstrom SiO_2 film which forms the etch mask for the trench etching. Next our Drytek poly-Si plasma etcher was used to obtain trenches 1.7 μ wide and 3.9 μ deep. The trenches have near vertical walls and a "U" shaped bottom. The tops of the trenches show a 0.3 μ undercut which indicates a vertical to horizontal etch ratio of 13. The trench etching conditions for the Drytek were: a pressure of 150 mTorr, a power density of 0.3 W/cm^2, an electrode temperature of 1 degree C, an SF_6 gas flow of 50 sccm, a C_2ClF_5 gas flow of 50 sccm, and an etch rate of 1950 Angstrom/min.

The next stage in this project will investigate the filling and backetch of these grooves using both deposited poly-Si and phosphorus doped oxide along with more plasma etching. Special emphasis will be placed on understanding and controlling parasitic channels which form near the walls of the trench.

4.4 Interconnections and Contacts

4.4.1 LPCVD of Tungsten

The equipment to do low pressure chemical vapor deposition (LPCVD) of tungsten was developed in collaboration with Tylan Corporation and installed in the IC Lab. Technology to do selective and non-selective homogeneous deposition of tungsten has been developed.

In the selective deposition process about 1000 to 2000 Angstroms of tungsten is deposited on exposed silicon *only* at temperatures around 400 degrees C. Currently contact resistance of LPCVD tungsten to n^+ and p^+ silicon is being characterized. This work will lead to reliable, low resistance self-aligned contacts to NMOS/CMOS circuits.

In the non-selective deposition technique thick (approx. 1.0 μ) films of tungsten have been deposited at temperatures around 400 degrees C on silicon with excellent mechanical integrity and resistivity approaching that of bulk tungsten. The adherence of these films to SiO_2 is very poor. Further work is required to develop a suitable "glue" metallurgy. Ti is being considered at this time. Once this technology is developed it may be possible to use thick films of W for interconnections.

4.4.2 Silicide Contacts

Silicide contacts to shallow n^+ and p^+ diffusions are being investigated in this project. The technology of PtSi contacts has been fully developed and utilized in the 2 μ CMOS process; whereas $TiSi_2$ contact technology is under development.

Thin films of Pt and TiW were deposited on <100> Si by sputtering, and the wafers were annealed at temperatures ranging from 400 to 800 degrees C in Ar. Formation of PtSi and $TiSi_2$ was studied by X-ray diffraction and auger electron spectroscopy. After determining the proper anneal conditions, test chips were fabricated to determine the contact resistance of PtSi/TiW/Al and TiW/Al structures to shallow and deep n^+ and p^+ junctions. The shallow junctions were similar to the ones used in our 2 μ CMOS process. Contact resistance was measured for different contact window size. The initial results indicate that $TiSi_2$ gives lower contact resistance to n^+ Si whereas PtSi gives lower contact resistance to p^+ regions by a small margin. This should be expected based on the barrier heights of Pt and Ti.

4.4.3 Planarization by Plasma Etching

Near the end of the fabrication process for standard integrated circuits the wafer surfaces have severe topologies which make the patterning and step coverage of the metal layers difficult. For a single level metal process this problem is usually overcome by depositing a thick layer of phosphorus doped SiO_2 (P-glass) over the whole wafer and then heating (1000 degrees C) In the past this high temperature step was compatible with standard CMOS process limitations.

An additional and more severe topology problem occurs when multi-level metal layers are used. For Al which is the dominant metal used, the P-glass flow method cannot be used to smooth the surface because the maximum temperature is limited to 450 degrees C which is well below any glass flow point. To solve this problem one can either go to a glass or insulator deposition process which is self-planarizing, i.e. smooths out and fills in the rough topology, or alternatively deposit a thick glass layer and then go through a planarizing step to get the desired surface topology. During this last period we have begun pursuing this second approach via plasma etching.

The planarization process which we are pursuing is to use the self-planarization of photoresist and then use plasma etching to replicate the planarized surface into a thick P-glass layer under the resist layer. The key to this process is the use of plasma etching to achieve equal etch rates for resist and P-glass.

Using a Drytek Model RIE-100 plasma etcher at 500 mTorr with a power of 0.4 W/cm_2 and a gas mixture of 28% O_2 in CF_4, etch rates for resist and P-glass (8% phosphorus) of 970 and 988 Angstroms/min, respectively, have been obtained. For a composite structure consisting of 1.0 micron of 180 degree C baked photoresist over 1.1 microns of P-glass deposited by LPCVD over a patterned poly-Si layer, planarization etching for 15 minutes resulted in smoothed-out P-glass surface. All valleys or low areas were partially filled in, depending on their width. For example a sharp 6000 angstrom high step in poly with a width of 5 microns was reduced to a rounded step only 2500 Angstroms high with a width of 3.3 microns. During the next period planarization technology will be looked at in more detail and applied to device fabrication.

4.4.4 Polyimides as Interlayer Dielectrics

The use of polymers for coatings and dielectrics is not a new science but recently the development of polymers and polyimides have led to their use in the ever expanding world of semiconductor electronics. In almost all semiconductor technologies there is the necessity to passivate active areas of devices or provide insulation using a dielectric between metallization patterns. The conventional techniques

previously used included the use of silicon dioxide, silicon nitride, silox, rotox and others for covering materials used in passivating techniques, as insulation between metallization and as masks for patterning. These materials suffer from several problems such as cracking, limited layer thicknesses, patterning problems, etc. which makes it desirable to find alternate materials with better properties. Due to the advances made in polymer sciences, polymers and polyimides are now challenging the conventional materials for their applications in semiconductor fabrication.

We have characterized DuPont's polyimide PI-2250 and Hitachi's photosensitive polyimide Ph-PIQ. The basic difference between the two materials is that a positive photoresist is needed on top of PI-2250 for pattern transfer from a mask, whereas Ph-PIQ is photosensitive and therefore the patterns can be directly defined in it directly by the process of photolithography. In this work we have characterized the formation of thin films of polyimides, effects of annealing on thickness and adhesion to the substrate, photolithography and etching to define fine patterns. Al/polyimide/Si capacitors were fabricated and the dielectric strength and ionic contamination were studied by the C-V technique.

In general this preliminary work indicates that both PI-2250 as well as Ph-PIQ can be used as an interlayer dielectric; however, further work is needed for their process implementation.

4.4.5 Plasma Etching of Contacts in SiO_2

Vertical walled contact windows in SiO_2 to a polysilicon gate, produced by reactive ion etching (RIE), are not suitable as a final structure in integrated circuit technology. This is due to the fact that vacuum deposited metals will not possess adequate coverage over vertical steps. A solution to this problem is to taper the sidewall of the etch pit so that the sidewall subtends a larger angle to the deposition source. One method of achieving sloped walls is by controlled photoresist erosion. If the photoresist has a slightly rounded profile before etching, the selectivity can be adjusted to produce sloped walls.

This study consisted of two parts. First, a matrix of experiments was designed to determine etch rates and uniformity of Si, SiO_2, and optical resist as a function of gas mixture, gas flow, pressure, and power. The gas mixture consisted of He, CHF_3, C_2F_6, and O_2. An important consideration was the selectivity between the etch rates of SiO_2 to Si in the event of overetch due to non-uniformities in the plasma.

With the RIE system used in this study (Branson/IPC, Hayward, CA), the etch rate, selectivity, and uniformity were optimized at flow rates of 2800 sccm He, 200 sccm CHF_3, and 220 sccm C_2F_6 at 10 Torr and 700 W power levels.

The second part of this study involved the RIE of patterned wafers using the above parameters. However, the resultant sidewall profiles were nearly vertical and some undercutting was evident. When O_2 was added to the gas mixture at flow rates up to 42 sccm, the result was an erosion of the resist and a tapering of the sidewall to an angle of approximately 70 degrees. However, selectivity was reduced from 10.8 to 2.4 due to oxidation of a polymeric layer that inhibited etching of Si. The operating parameters were thus modified to maximize selectivity.

It was found from these studies that the sidewall profile was largely dependent on the selectivity of SiO_2 to resist etch rates. At high selectivities, vertical profiles resulted. As the selectivity approached one, sloped profiles, adequate for VLSI, resulted.

4.4.6 Interconnection Test Mask

A design for a mask set involving five layers of interconnections has been completed. This mask set is designed in a manner such that any subset of the five layers can be used. An additional feature of the mask set is that in addition to having test structures for the current 4 micron wet etching process, there are test structures for two-micron and one-micron technologies.

The test structurs included in this design range from snake patterns to test step coverage to Kelvin contacts to measure interfacial contact resistance. There are also contact strings with several thousand contacts for each of the three technologies, capacitors between each layer to test the dielectric integrity, and other "standard" test structures (resistivity, line widths, long lines for SEM cross sections).

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